4H-SiC Power Schottky diodes. On the way to solve size limiting issues.

A. Syrkin(1), V. Dmitriev(1), M. Mynbaeva(2), C. Hallin(3), and E. Janzén(3)

(1) TDI, Inc. 12214 Plum Orchard Dr., Silver Spring, MD 20904, USA
(2) Ioffe Physical-Technical Institute, Russian Academy of Sciences, Polytechnicheskaya 26, 194021, St Petersburg, Russia
(3) Linköping University, IFM, S-581 83 Linköping, Sweden
Ph.:+1-(301)-572 7834; Fax:+1-(301)-572 6435; e-mail: asyrkin@tdii.com

In this paper we report on experimental results in solving defect-related issues limiting the size and performance of 4H-SiC based power Schottky diodes. Several techniques improving wafer quality were used in line to fabricate power Schottky diodes with high current capability for blocking voltage over 600 V. Results of X-ray investigation of wafers on every step of treatment from initial wafer to template with diode base layer with corresponding improvement of structural quality is reported. Ways of defects density reducing are discussed and compared. Results on 5 mm diameter 4H-SiC Schottky diodes fabrication and characterization are reported. The on–state resistance as low as 0.07 Ω is demonstrated. Corresponding forward voltage drop at 50 A is estimated to be 5 V.
4H-SiC Power Schottky diodes. On the way to solve size limiting issues.

A. Syrkin(1), V. Dmitriev(1), M. Mynbaeva(2), C. Hallin(3), and E. Janzén(3)

(1)- TDI, Inc. 12214 Plum Orchard Dr., Silver Spring, MD 20904, USA
(2)- Ioffe Physical-Technical Institute, Russian Academy of Sciences, Polytechnicheskaya 26, 194021, St Petersburg, Russia
(3)- Linköping University, IFM, S-581 83 Linköping, Sweden
Ph.:+1-(301)-572 7834; Fax:+1-(301)-572 6435; e-mail: asyrkin@tdii.com

Schottky diode is considered to be one of the most attractive power devices in silicon carbide. Despite the strong effort of several teams over the world there is still no commercial Schottky device capable to handle even 100 A in a single chip. The limit of on-state operation for SiC based Schottky diodes is set by insufficient material quality to provide the required blocking capability for the diode of appropriate size.

In this paper we report on experimental results in solving defect related issues limiting SiC Schottky diode area. Combination of two technologies was used to reduce the size–limiting defects density. Micropipe-filling technique was employed using preliminary anodised 4H-SiC commercial wafer providing porous buffer layer under the filling layer. Low doped epitaxial layer was then grown by CVD method. Initial wafer, micropipe filled layer and CVD layer were subsequently investigated using X-ray diffraction. We measured ω-scan X-ray rocking curves using low angle (0004) symmetrical reflection method. Substantial improvement of structural quality is demonstrated for epitaxial layer grown on the wafer with reduced defect density Fig.1.

Gold plated Ni–based 5 mm diameter 4H-SiC Schottky diode with on-state resistance of 0.07 Ω and blocking voltage of 600V are demonstrated using wafers with reduced defect density. We made an analysis of on-state resistance terms including backside ohmic contact, wafer in-series resistance, buffer layer resistance and base layer resistance. The contribution of base region and contacts in the on-state diode resistance defined the diode forward characteristics. Porous buffer layer apparently may as well affect the on-state resistivity of the diode structure. The calculated level of diode resistance for 5 mm diameter diode was 0.046 Ω, that is slightly below estimation obtained based on measured values. Effect of measurement circuit resistance on measurement results for large area diodes is clearly seen (Fig 2). We expect to handle currents up to 50 A in single chip at forward drop of 5V for reported diodes after proper packaging.

We will discuss possible ways of further improvement of SiC crystal quality and Schottky diodes performance.

This work is supported in part by the OSD through the Office of Naval Research, contract N00014-03-M-0055, contract monitor Kristl Hathaway.
Fig. 1. Rocking curves for the (0004) reflection, ω-scan, for 4H-SiC commercial wafer, the same wafer after micropipe filling, and the same wafer with CVD active layer.

Fig. 2. Dependence of on–state resistance for 4H-SiC Schottky diode on diode area.
For 4H-SiC(11-20), the electrical activation process of the implanted phosphorus in the layer regrown from the amorphized implant-layer is investigated by Rutherford backscattering spectrometry and Hall effect measurement. To form the implant-layer with a phosphorus concentration of $2 \times 10^{21}$ /cm$^3$ and a thickness of 120 nm, the samples were implanted by phosphorus ions with a total dose of $1.4 \times 10^{16}$/cm$^2$ at room temperature. The amorphous layer is recrystallized by annealing at 1000 °C for 30 min, which is correlated to the rapid crystallization of implanted layer in SiC(11-20). The sheet carrier concentration of $2.4 \times 10^{15}$/cm$^2$ is obtained by annealing at 1000 °C for 30 min. It is suggested that the solid-phase epitaxy process of amorphized implant-layer promotes the substitution of the implanted phosphorus on the host SiC lattice sites. The minimum sheet resistance of 190 ohm-cm$^2$ is achieved by annealing at 1500 °C for 5 min while the implanted phosphorus is diffused out from the surface during the recrystallization of the amorphous layer.
STUDY OF PHOSPHORUS IMPLANTED 4H-SiC(11-20)

M. Satoh, T. Hitomi, S. Katagami, and T. Nakamura
Research Center of Ion Beam Technology and College of Engineering, Hosei University, Koganei Tokyo 184-8584, Japan
Phone: +81-42-387-6091, Fax: +81-42-387-6095, E-mail: mah@ionbeam.hosei.ac.jp

The implantation-induced amorphous layer in the SiC(11-20) is rapidly crystallized in accordance to the crystalline structure of the underlying substrate. It is expected that the amorphization of the implanted layer in SiC(11-20) promotes the highly electrical activity of the implanted impurities and the reduction of the annealing temperature. It has been reported that the implanted phosphorus is sufficiently activated by annealing even though the as-implanted layer contains a large amount of defects or is amorphized[1,2]. However, there is a few study about the electrical activation process of the implanted phosphorus in the layer regrown from the amorphized implant-layer in SiC(11-20) [2].

In this study, we report that the structural and electrical properties of the phosphorus-implanted layer with a concentration of the order of \(10^{21} / \text{cm}^3\) in 4H-SiC(11-20).

Samples used in this study were p-type 4H-SiC(11-20) with a carrier concentration of the order of \(10^{14} / \text{cm}^3\), which is provided from Nippon Steel Co. Wafers were cut from the (0001)-oriented ingots grown by sublimation method. To form the implanted layer with a maximum phosphorus concentration of \(2 \times 10^{21} / \text{cm}^3\) and a thickness of 120 nm, the samples were multiply implanted by phosphorus ions with energies of 50 and 100 keV at doses of \(4 \times 10^{15}\) and \(1 \times 10^{16} / \text{cm}^2\) (total dose = \(1.4 \times 10^{16} / \text{cm}^2\)), respectively, at room temperature. The annealing of samples was performed in temperature range from 1000 to 1500 °C for 5-30 min in a flow of Ar gas using an inerfered annealer with a black SiC crucible. The crystalline quality of the implanted layer was evaluated by Rutherford backscattering spectrometry (RBS) using a 1.5 MeV \(^{4}\text{He}\) beam. The electrical properties of the implanted layer was investigated by means of Van de Pauw and Hall effect measurements. The depth profile of the implanted phosphorus was evaluated by secondary ion mass spectrometry.

Figure 1 shows RBS spectra taken from implanted sample before and after annealing at 1000 °C for 30 min. In the as-implanted sample, the amorphous layer with a thickness of 120 nm is formed by implantation. In the sample annealed at 1000 °C for 30 min, the normalized minimum yield (\(X_{\text{min}}\)) at a depth beyond the surface peak is estimated to be 4.3 %. For the sample annealed at 1500 °C for 30 min, \(X_{\text{min}}\) value was 2.7 %. The good crystalline quality of the implanted layer is correlated to the epitaxial regrowth of amorphous layer. The maximum of yield observed around 260 channel in RBS spectrum for the annealing temperature of 1000 °C is originated from the end-of-range-damage, which is removed by annealing above 1200 °C. Figure 2 shows the annealing temperature dependence of sheet carrier concentration and sheet mobility. The highest sheet carrier concentration of \(2.4 \times 10^{15} / \text{cm}^2\) is obtained by annealing at 1000 °C for 30 min. It is suggested that the implanted phosphorus impurities easily occupy the lattice sites without migrating during the re-crystalliation process of SiC host lattice. The low carrier mobility in samples annealed at 1000 and 1200 °C is arisen from the existence of the defects extended from the interface between implanted layer and substrate, which is annealed out by annealing at 1500 °C. As the sample is annealed at 1500 °C,
however, the sheet carrier concentration was decreased to $1 \times 10^{15}$ /cm$^2$ while there is no annealing-time dependence of sheet carrier concentration. The sheet resistance was 190 ohm-cm$^2$. Figure 3 shows the depth profile of phosphorus before and after annealing at 1500 °C for 10 min. The decrease of the phosphorus concentration and the large redistribution of phosphorus were observed. Such phenomenon was not observed for the sample implanted at 500 °C(not shown). It is strongly suggested that the implanted phosphous is duffused out from the surface in the initial stage of the recrystallization of the amorphous layer.

We have investigated the SiC/Si multilayer formation on Si(100) by supersonic free jet CVD utilizing single gas source, CH$_3$SiH$_3$. The CVD chamber was equipped with mechanical and turbomolecular pumps and had a base pressure of $\sim$10$^{-6}$ Torr. The H$_2$ diluted 10\% CH$_3$SiH$_3$ gas was introduced into the chamber by using a pulse valve with a nozzle diameter of 0.8 mm. A tungsten hot filament set at $\sim$1800 °C was placed in front of the Si substrate for the Si growth. The substrate temperatures during the SiC and Si growths were 850 °C and 500 °C, respectively. The crystallinity and the morphology of the SiC/Si multilayers were characterized by cross-sectional transmission electron microscopy measurements.

When the CH$_3$SiH$_3$ jets were irradiated for 18000 pulses during the SiC and Si growths, the crystalline spots corresponding to epitaxially grown 3C-SiC on Si(100) and a weak halo pattern indicating amorphous Si were seen in the diffraction pattern. In the bright-field image, the amorphous Si layer was grown on epitaxial 3C-SiC/Si(100). The thicknesses of the epitaxial SiC and the amorphous Si layers were 15 and 30 nm, respectively. These results suggest that SiC/Si multilayer structures can be grown by using single gas source CH$_3$SiH$_3$. 
Si-based semiconductor multilayer heterostructures are very important for applications to quantum devices such as resonant tunneling diodes (RTDs). Si-based RTDs have been mainly studied using Si/SiGe heterostructures [1]. However, the peak-to-valley current ratio is still low comparing with GaAs-based RTDs.

Cubic 3C-SiC is a wide band gap (2.2 eV) semiconductor and can be epitaxially grown on Si substrates. Since the 3C-SiC/Si(100) interface has wider valence and conduction band offsets than those of Si/SiGe [2], the 3C-SiC/Si heterostructures may be more attractive for fabrications of Si-based quantum devices. Recently, we have reported the formation of 3C-SiC/Si multilayers [3,4] and SiC/Si-dot/SiC heterostructures [5,6] by supersonic free jet CVD using CH$_3$SiH$_3$ and Si$_3$H$_8$ gas jets. In this study, we have investigated the SiC/Si multilayer formation by supersonic free jet CVD utilizing single gas source CH$_3$SiH$_3$. The crystallinity and the morphology of the SiC/Si multilayers were characterized by cross-sectional transmission electron microscopy (XTEM).

The CVD chamber was equipped with mechanical and turbomolecular pumps and had a base pressure of ~$10^{-8}$ Torr. The H$_2$ diluted 10% CH$_3$SiH$_3$ gas was introduced into the chamber by using a pulse valve with a nozzle diameter of 0.8 mm. A tungsten hot filament set at ~1800 °C was placed in front of the Si substrate for the Si growth. The substrate temperatures during the SiC and Si growths were 850 °C and 500 °C, respectively. The CH$_3$SiH$_3$ pulse width and frequency were set at 130 µs and 10 Hz, respectively.

Figures 1(a) and 1(b) show the XTEM bright-filed image and diffraction pattern obtained from the sample grown by CH$_3$SiH$_3$ jet irradiations of 18000 pulses during the SiC and Si growths. The diffraction spots corresponding to epitaxially grown 3C-SiC on Si(100) and a weak halo pattern indicating amorphous Si can be seen in the diffraction pattern. In the bright-field image, the amorphous Si layer is grown on epitaxial 3C-SiC/Si(100). The thicknesses of the epitaxial SiC and the amorphous Si layers are 15 and 30 nm, respectively. These results suggest that SiC/Si multilayer structures can be grown by using single gas source CH$_3$SiH$_3$.

Fig. 1 (a) XTEM diffraction pattern and (b) bright-field image of Si/3C-SiC/Si(100). The amorphous Si layer is grown on the epitaxial 3C-SiC film.
Formation of SiC/Si multilayer structures on Si(100) by supersonic free jets of single gas source CH$_3$SiH$_3$

Yoshifumi Ikoma, Ryota Ohtani, and Teruaki Motooka
Department of Materials Science and Engineering, Kyushu University
6-10-1 Hakozaki, Fukuoka 812-8581, Japan
Tel: +81-92-642-3677, Fax: +81-92-632-0434, e-mail: ikoma@zaiko.kyushu-u.ac.jp

We have investigated the SiC/Si multilayer formation on Si(100) by supersonic free jet CVD utilizing single gas source, CH$_3$SiH$_3$. The CVD chamber was equipped with mechanical and turbomolecular pumps and had a base pressure of ~10$^{-8}$ Torr. The H$_2$ diluted 10% CH$_3$SiH$_3$ gas was introduced into the chamber by using a pulse valve with a nozzle diameter of 0.8 mm. A tungsten hot filament set at ~1800 °C was placed in front of the Si substrate for the Si growth. The substrate temperatures during the SiC and Si growths were 850 °C and 500 °C, respectively. The crystallinity and the morphology of the SiC/Si multilayers were characterized by cross-sectional transmission electron microscopy measurements.

When the CH$_3$SiH$_3$ jets were irradiated for 18000 pulses during the SiC and Si growths, the crystalline spots corresponding to epitaxially grown 3C-SiC on Si(100) and a weak halo pattern indicating amorphous Si were seen in the diffraction pattern. In the bright-field image, the amorphous Si layer was grown on epitaxial 3C-SiC/Si(100). The thicknesses of the epitaxial SiC and the amorphous Si layers were 15 and 30 nm, respectively. These results suggest that SiC/Si multilayer structures can be grown by using single gas source CH$_3$SiH$_3$. 
Formation of SiC/Si multilayer structures on Si(100) by supersonic free jets of single gas source CH$_3$SiH$_3$

Yoshifumi Ikoma, Ryota Ohtani, and Teruaki Motooka
Department of Materials Science and Engineering, Kyushu University
6-10-1 Hakozaki, Fukuoka 812-8581, Japan
Tel: +81-92-642-3677, Fax: +81-92-632-0434, e-mail: ikoma@zaiko.kyushu-u.ac.jp

Si-based semiconductor multilayer heterostructures are very important for applications to quantum devices such as resonant tunneling diodes (RTDs). Si-based RTDs have been mainly studied using Si/SiGe heterostructures [1]. However, the peak-to-valley current ratio is still low comparing with GaAs-based RTDs.

Cubic 3C-SiC is a wide band gap (2.2 eV) semiconductor and can be epitaxially grown on Si substrates. Since the 3C-SiC/Si(100) interface has wider valence and conduction band offsets than those of Si/SiGe [2], the 3C-SiC/Si heterostructures may be more attractive for fabrications of Si-based quantum devices. Recently, we have reported the formation of 3C-SiC/Si multilayers [3,4] and SiC/Si-dot/SiC heterostructures [5,6] by supersonic free jet CVD using CH$_3$SiH$_3$ and Si$_3$H$_8$ gas jets. In this study, we have investigated the SiC/Si multilayer formation by supersonic free jet CVD utilizing single gas source CH$_3$SiH$_3$. The crystallinity and the morphology of the SiC/Si multilayers were characterized by cross-sectional transmission electron microscopy (XTEM).

The CVD chamber was equipped with mechanical and turbomolecular pumps and had a base pressure of ~10$^{-8}$ Torr. The H$_2$ diluted 10% CH$_3$SiH$_3$ gas was introduced into the chamber by using a pulse valve with a nozzle diameter of 0.8 mm. A tungsten hot filament set at ~1800 °C was placed in front of the Si substrate for the Si growth. The substrate temperatures during the SiC and Si growths were 850 °C and 500 °C, respectively. The CH$_3$SiH$_3$ pulse width and frequency were set at 130 µs and 10 Hz, respectively.

Figures 1(a) and 1(b) show the XTEM bright-filed image and diffraction pattern obtained from the sample grown by CH$_3$SiH$_3$ jet irradiations of 18000 pulses during the SiC and Si growths. The diffraction spots corresponding to epitaxially grown 3C-SiC on Si(100) and a weak halo pattern indicating amorphous Si can be seen in the diffraction pattern. In the bright-field image, the amorphous Si layer is grown on epitaxial 3C-SiC/Si(100). The thicknesses of the epitaxial SiC and the amorphous Si layers are 15 and 30 nm, respectively. These results suggest that SiC/Si multilayer structures can be grown by using single gas source CH$_3$SiH$_3$.

Fig. 1 (a) XTEM diffraction pattern and (b) bright-field image of Si/3C-SiC/Si(100). The amorphous Si layer is grown on the epitaxial 3C-SiC film.
Low sheet resistance of aluminum-ion implanted 4H-SiC using (11-20) face

Yuuki NEGORO, Kazunari KATSUMOTO, Tsunenobu KIMOTO, and Hiroyuki Matsunami
Department of Electronic Science and Engineering, Kyoto University, Yoshidahonmachi, Sakyo, Kyoto, 606-8501, Japan.
Tel: +81-75-753-5341, Fax: +81-75-753-5342, E-mail: negoro@semicon.kuee.kyoto-u.ac.jp

High-dose aluminum-ion (Al⁺) implantation into 4H-SiC (11-20) has been investigated for the first time. The total implant-dose of Al⁺ was varied from $4.0 \times 10^{15}$ cm⁻² to $6.0 \times 10^{16}$ cm⁻², which corresponds to the Al concentration from $2.0 \times 10^{20}$ cm⁻³ to $3.0 \times 10^{21}$ cm⁻³. Some of the samples were prepared by utilizing co-implantation of carbon-ion (C⁺). All implantations were carried out at 500°C. Post implantation annealing was performed in an Ar ambience at 1800°C using a CVD reactor. Electrical properties of implanted SiC were measured by Hall effect using the van der Pauw configuration. In the case of Al⁺ implantation into (11-20), the sheet resistance could be reduced to 1.9 kΩ/sq. (p-type) by increasing the implant-dose up to $6.0 \times 10^{16}$ cm⁻². This is the lowest value ever reported. The Hall-mobility (hole) strongly differs in (11-20) and (0001). The mobility in (11-20) takes 7.2 cm²/Vs at RT, which is about 3 times higher than that in (0001). The temperature dependence of free hole concentration for each face is extremely weak. Annealing time dependence of sheet resistance, SIMS profile, and surface morphologies of Al⁺-implanted 4H-SiC (11-20) and (0001) will be discussed.
Ion implantation, an indispensable technique to locally dope SiC, still has problems, in particular, for forming p⁺-SiC with a low sheet resistance. Although high-dose Al⁺ implantation at an elevated temperature and subsequent annealing at 1800°C have been used for forming p⁺-SiC [1], the sheet resistances of p⁺-SiC are still not low enough to use for real power devices. The (11-20) face has shown various promising properties such as a superior MOS interface [2] and a low sheet resistance of P⁺-implanted region [3]. However, no reports have been published on high-dose Al⁺ implantation into 4H-SiC (11-20). Different characteristics of Al⁺-implanted SiC can be expected by using different faces. In this study, the authors present the characteristics of high-dose Al⁺-implanted 4H-SiC (11-20).

N-type 4H-SiC (0001) and (11-20) epitaxial layers with a net donor concentration of $1.0 \times 10^{16}$ cm⁻³ grown in the authors' group were used in this study. Multiple implantation of Al⁺ (10-160 keV) was carried out at 500°C to obtain a 0.2 μm-deep box profile of Al. In this study, the total implant-dose was varied from $4.0 \times 10^{15}$ to $6.0 \times 10^{16}$ cm⁻², which corresponds to the Al concentration from $2.0 \times 10^{20}$ to $3.0 \times 10^{21}$ cm⁻³. Some of the samples were prepared by utilizing co-implantation of C⁺ with a 20% dose of implanted Al⁺. Post implantation annealing was performed in an Ar ambience at 1800 °C using a CVD reactor. The electrical properties of implanted regions were characterized by Hall effect measurements using the van der Pauw configuration.

Figure 1 shows the implant-dose dependence of sheet resistance for Al⁺-implanted 4H-SiC (0001) and (11-20). In the case of Al⁺ implantation into (0001), the sheet resistance takes the minimum value of 2.9 kΩ/sq., at an implant-dose of $3.0 \times 10^{16}$ cm⁻². This is comparable to recent reports [1]. The sheet resistance for (0001) samples turns to increase, when the implant-dose exceeds $3.0 \times 10^{16}$ cm⁻². When C⁺ co-implantation was employed, sheet resistances were reduced by 3-20% compared to those of only Al⁺ implantation. In the case of (11-20), the sheet resistance could be reduced to 1.9 kΩ/sq. by increasing the implant-dose up to $6.0 \times 10^{16}$ cm⁻². This is the lowest value ever reported. In terms of C⁺ co-implantation into (11-20), a tendency of sheet resistance was similar to (0001).

Figure 2 shows the temperature dependence of Hall-mobility (hole) for Al⁺/C⁺ co-implanted (0001) and (11-20). Implant-doses are $3.0 \times 10^{16}$ cm⁻² of Al⁺ and $6.0 \times 10^{15}$ cm⁻² of C⁺. The mobility strongly differs in (0001) and (11-20). The mobility in (11-20) takes 7.2 cm²/Vs at RT, which is about 3 times higher than that in (0001).

Figure 3 shows the free hole concentration $p$ as a function of the reciprocal temperature obtained from Hall effect measurements on the Al⁺/C⁺ co-implanted (0001) and (11-20). The lower $p$ for (11-20) may be attributed to the out-diffusion of Al atoms during high-temperature annealing, which is revealed by SIMS measurements. The suppression of the out-diffusion of implanted Al atoms in (11-20) may lead to the further reduction of sheet resistance in (11-20).

Annealing time dependence of sheet resistance, SIMS profile, and surface morphologies of Al⁺-implanted 4H-SiC (0001) and (11-20) will be discussed.
References


Fig. 1. Implant-dose dependence of sheet resistance for Al<sup>+</sup> with/without C<sup>+</sup> co-implanted 4H-SiC (0001) and (11-20).

Fig. 2. Hall-mobility (hole) vs. temperature characteristics for Al<sup>+</sup>/C<sup>+</sup>-implanted 4H-SiC (0001) and (11-20).

Fig. 3. Free hole concentration as a function of reciprocal temperature for Al<sup>+</sup>/C<sup>+</sup>-implanted 4H-SiC (0001) and (11-20), where \( N_v \) is the effective density of states in the valence band.
We report on the design, fabrication, testing and analysis of 4H-SiC bipolar junction transistors with power dissipation density up to 4.9 MW/cm$^2$ and operation up to 500°C. This record power density is attributed to the high thermal conductivity of the SiC and the ability to operate at high junction temperature. The junction temperature was extracted from the measured common emitter I-V characteristics at ambient temperatures of 35°C, 65°C and 95°C. We found that the junction temperature can be well fitted to a simple heat conduction model.
SiC is endowed with high thermal conductivity, a wide bandgap and high breakdown field and is therefore of interest for high-power and high-temperature transistors. High-power dissipation density and high-temperature operation is advantageous for a wide range of applications. High power dissipation density translates in higher power handling capability, which is useful for both power switching and RF power applications as both types of devices tend to be limited by the removal of heat. While operation at record temperature is not necessarily of interest due to reduced performance and reliability with increasing temperature, higher temperature operation at junction temperature up to 200°C does facilitate heat removal. It also shows the transistor’s tolerance to temporary overheating in harsh and uncontrollable environments.

In this paper we describe 4H-SiC Bipolar Junction Transistors with up to $4.9 \text{MW/cm}^2$ DC power dissipation density and present a simple thermal model which predicts the junction temperature of SiC bipolar transistors under both self-heating conditions and while operating at high ambient temperatures. The device is fabricated by dry etching a double-mesa structure as described in reference [1]. The structure was subsequently passivated, followed by the deposition of the emitter/collector metal and the base metal. A second isolation layer and wiring metal then completed the device fabrication. Figure 1 shows a schematic of the finished device.

The devices were tested from room temperature up to 500°C in steps of 50 degrees or less. Current-voltage, Gummel plots and diode characteristics were recorded at each temperature. As an example, we present the $I-V$ characteristics comparing a device at 35°C and 400°C. The junction temperature was extracted from $I-V$ characteristics following the method of Marsh [2]. The junction temperature was found to be super-linear with power dissipation, which is consistent with a decreasing thermal conductivity with increasing temperature. Figure 3 shows the good agreement between the extracted and calculated junction temperature. The calculated junction temperature was obtained with a simple thermal model that will be presented in detail.

More detailed electrical DC characteristics are presented in figure 4. The peak current and power density of this device are 185 kA/cm² and 4.9 MW/cm², both record values for any SiC BJT. As expected under these extreme conditions the resulting $I-V$ curves exhibit self-heating and gain compression. The high current density exposes the high base resistance of the devices with a distinct turn-on voltage. Using the thermal model described above we find that the corresponding junction temperature is well above 600°C. The high junction temperature and record power dissipation density are both testimony of the superior high temperature operation and heat removal of SiC BJTs.

This work was supported in part by AFRL, program monitor John King (Wright Patterson Air Force Base)
Figure 1 Cross section of the double mesa BJT structure

Figure 2 $I-V$ Characteristics of a 10 x 80 $\mu$m device a) at 35°C with $I_B = 0.15, 0.3, 0.45, 0.6,$ and 0.75 mA, b) at 400°C with $I_B = 0.25, 0.5, 0.75, 1.0,$ and 1.25 mA.

Figure 3 Extracted (markers) and calculated (solid lines) junction temperature versus power dissipation for an ambient temperature of 95°C (left), 65°C, and 35°C (right).

Figure 4 $I-V$ curves of a 3 x 10 $\mu$m$^2$ device at room temperature with a base current of 1, 2, 3, 4, 5, 6, and 7 mA.