Available online at www.sciencedirect.com
ScienceDirect
Nuclear Instruments and Methods in Physics Research A 572 (2007) 333–334
NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH Section A
www.elsevier.com/locate/nima

PAMELA Data Acquisition System

Alessandro Basili

INFN sez.di Roma Tor Vergata, 00133 Rome, Italy

on the behalf of the PAMELA Collaboration

Available online 30 November 2006

Abstract

The PAMELA experiment is a satellite-borne telescope primarily thought to explore the antimatter component of the cosmic rays. The instrument core is a permanent magnet surrounded by several instruments with different issues. Besides the TOF (Time-of-Flight), spectrometer, calorimeter, an anticoincidence system and a neutron detector, the experiment has an on-board computer responsible of the whole acquisition and housekeeping. In this work we will show the Data Acquisition flux for PAMELA, explaining the read-out mechanism from the Front End to the on-board CPU.

Keywords: PAMELA; Date aquistion system

1. Introduction

PAMELA telescope is a space born experiment for the cosmic rays exploration [1]. Composed by a Magnetic Spectrometer, an Anticounter System, a Time-of-Flight System, which also gives the trigger to the experiment, an Electromagnetic Imaging Calorimeter, a bottom scintillator called S4 and a Neutron Detector, it can identify particles within a wide energy range (80 MeV–190 GeV for antiprotons and 80 MeV–700 GeV for protons) and it is estimated that the AntiHelium/Helium sensitivity will reach up to 3×10^{-8} during the three years mission.

It will be mounted in a pressurized vessel attached to a Russian Earth-observation satellite, the Resurs DK1, that will be launched into space by a Soyuz TM2 rocket in June 2006 from Baikonur cosmodrome, in Kazakhstan. The orbit will be elliptical and semi-polar, with an inclination of 70.4 and an altitude varying from 350 to 600 km.

2. Data reduction chain

The data acquisition is handled by a SPARC32 V7 space qualified processor [2], which is interfaced with a 2×2 GB Solid State Mass Memory for data storing and a Mil-Std 1553 to communicate with the hosting satellite. Moreover, two dedicated interfaces have been implemented (House Keeping Unit and Parallel InterFace module) to handle the data taking.

The detector has more then 40 000 analog channels to be read, that is why has it been chosen as a data reduction approach. The system has an interface board (IDAQ) to multiplex out the commands from the Pamela Storage and Control Unit (PSCU) and to store the data from the DSP boards in the Mass Memory. These collect the digitized data from the Front End boards, on which the Analog-to-Digital Converter is located.

A trigger-busy approach is needed to handle each event and a DMA solution helps the data acquisition procedure with little cpu-time consuming. In fact, as the IDAQ releases the busy signal on the specific cpu command, the whole command queue is pending until a trigger is delivered by the trigger system. Monitoring the busy line status, the trigger system has the capability to measure the dead and live time of the acquisition, estimated to have a mean value of 100 ms.

All the DSP boards have their computational time to process the event, that is why an hardware timeout is implemented on the IDAQ, so that the whole acquisition procedure is completely handled by this board with practically no cpu time consuming. Meantime the cpu can monitor all the housekeeping alarms and status in order to recover a faulty condition as soon as possible.

E-mail address: alessandro.basili@roma2.infn.it.

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doi:10.1016/j.nima.2006.10.337

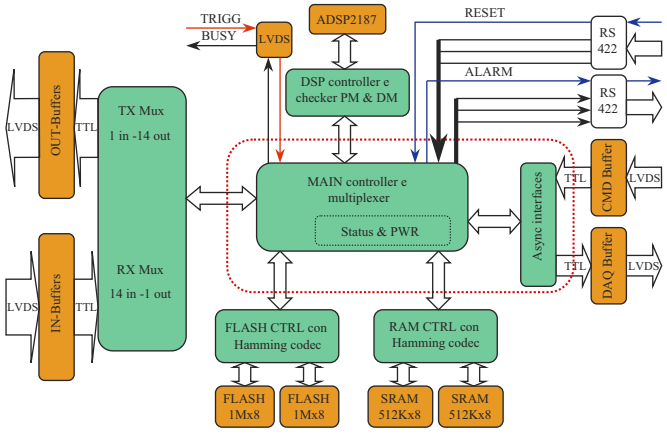

Fig. 1. IDAQ functional block scheme.

3. Interface Data Acquisition board

The Interface Data Acquisition board is an Actel FPGA based board, with a second-level handshake protocol with the PSCU and a Data-Strobe protocol with the readout boards.

There are five FPGAs, one is the main controller, which is the master, while the others handle the interface with the Front End boards, the Ram, the Flash and the DSP which act as slaves (see Fig. 1). The external I/O are LVDS standard to guarantee the minimum cross-talk and ensure a correct data flux. The board is equipped with a DSP (Analog Device ADSP2187L), a RAM memory (CY62146V 4 Mb Static RAM CYPRESS) and a FLASH memory (Am29LV800B 8 Mb, AMD) for the second level trigger and for data buffering on board, in case of multiple event acquisition. Both the Ram and the Flash devices have a Cyclic Redundancy Checker to recover single bit error and to set an alarm in case of double bit fault. The DSP is set in IDMA configuration and from the command queue point of view all the addressing overlays are handled by the controller which shows DSP memory as a linear 32 KWord (overlay equal to 1, 4 and 5).

First level trigger has different selectable configurations which involve the TOF system, calorimeter and S4. Second level trigger is needed to reduce cases of big amount of not valid data (an 80% of data are estimated to be out of the acceptance). This algorithm needs to check the anticounter and calorimeter data to cut out the event because backscattering can happen in the calorimeter and the anticounter data only would not be enough.

4. DSP boards

All the DSP boards host an ADSP2187L processor with a single-cycle instruction execution and a 52 MIPS sustained performance. Its 160 K bytes on-chip ram allows fast data processing with low power consumption, moreover it has been tested for total-dose and rad-hard conditions [3] to guarantee reliability operation in-flight.

DSP boards have been chosen to minimize the total amount of data with compression algorithms on the raw data acquired from the Front End boards and to minimize the total number of commands sent by the CPU.

For instance, while the TOF system utilizes the DSP to pack the data without compression (few bytes), Calorimeter and Tracker systems needed to develop a dedicated compression algorithm for the large amount of data read. AntiCounter uses it to calibrate the detector, varying discriminators threshold and checking the status.

The tracking system has implemented a Zero Order Predictor with a clusters finder algorithm. In this way only data above a certain value will be stored and it is clear that this cut has to be defined relatively to the pedestal signal. This is the reason why an iterative algorithm is needed to identify the pedestal, which include common noise and single channel noise that are evaluated with several "pedestal run" during the acquisition time. Considering that the total amount of data collected from the VA1 chip are 55 KB, it is clear the importance of data processing. The compression ratio is estimated to be 95% without any worsening in spatial and momentum resolution of the detectors.

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