

The PAMELA storage and control unit

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Abstract

The PAMELA Storage and Control Unit (PSCU) comprises a Central Processing Unit (CPU) and a Mass Memory (MM). The CPU of the experiment is based on a ERC-32 architecture (a SPARC v7 implementation) running a real time operating system (RTEMS). The main purpose of the CPU is to handle slow control, acquisition and store data on a 2 GB MM. Communications between PAMELA and the satellite are done via a 1553B bus. Data acquisition from the sub-detectors is performed via a 2 MB/s interface. Download from the PAMELA MM towards the satellite main storage unit is handled by a 16 MB/s bus. The maximum daily amount of data transmitted to ground is about 20 GB.

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1. Introduction

The scientific goals of PAMELA [1] are the accurate measurements of the antiproton and positron fluxes with a sensitivity and statistics out of the reach of most previous (mainly balloon-borne) experiments, and the search for possible antinuclei, with a sensitivity better than 10^{-7} in the antihelium-to-helium ratio. For its characteristics PAMELA will also address several issues of solar and heliospheric physics [2]. The investigated energy range goes from below 100 MeV to some hundreds of GeV. The PAMELA telescope will be installed on board of the Russian Resurs DK-1 satellite and will be launched in the year 2005. The experiment is designed in an hierarchical/modular structure where the subdetectors handle all fast acquisition and data suppression before sending data to the acquisition board that

interfaces them to the CPU. Then, data are stored into the MM before transfer to the satellite. The intermediate boards have all their redundancy and all detectors are divided in sections designed to continue working—although with degraded performances—even in case of partial failures (Fig. 1).

2. The PSCU

The PAMELA Storage and Control Unit handles all slow controls, the interactions between the satellite, and the data acquisition, storage and downlink.

It is a space qualified system composed of (Fig. 2):

- a central processor ERC32 SPARC V7 with a clock of 24 MHz employing a PROM of 128 KB for booting, 4 MB of RAM, and two 512 kB banks of EEPROM;
- an avionics standard 1553B BUS interface board from/ to the Resurs satellite.

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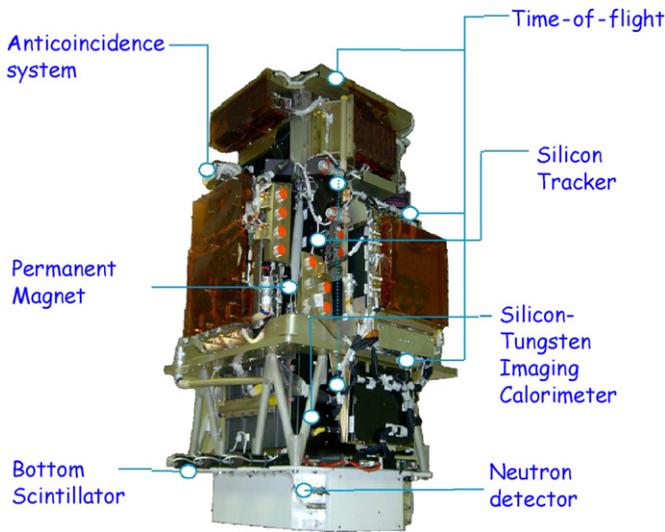


Fig. 1. The PAMELA detector with its various subsystems.

- a multipurpose TeleMetry and Control board (TMTC) containing various digital, ADC/DAC interfaces to interact with the subdetectors and the subsystems of the experiment.

References

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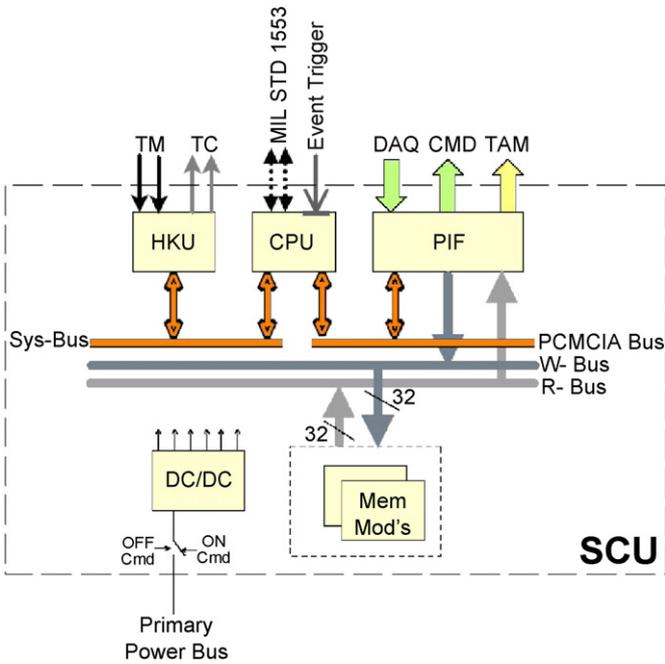


Fig. 2. Block scheme of the CPU.

- two mass memory modules, 1 GB each, used to store all data coming from the Front End boards.
- a high speed interface board to issue commands/receive data from subdetectors.