



ELSEVIER

Available online at www.sciencedirect.com

SCIENCE @ DIRECT®

Nuclear Instruments and Methods in Physics Research A 518 (2004) 161–163

NUCLEAR
INSTRUMENTS
& METHODS
IN PHYSICS
RESEARCH
Section A

www.elsevier.com/locate/nima

The ToF and Trigger electronics of the PAMELA experiment

G. Osteria^{a,*}, G. Barbarino^a, M. Boscherini^b, D. Campana^a, P. Di Meo^a,
M. Di Pietro^a, W. Menn^b, M. Orazi^a, R. Rocco^a, M. Simon^b, E. Weber^a

^a *Università "Federico II" and INFN sez. di Napoli, Napoli 80126, Italy*

^b *Universität-GH Siegen, FB Physik, Siegen 57068, Germany*

Abstract

The PAMELA satellite-borne experiment, scheduled to be launched in 2004, is designed to provide a better understanding of the antimatter component of the cosmic rays. Its ToF scintillator system will provide the primary experimental trigger and time-of-flight particle identification. The time resolution requested is $\sigma_t < 120$ ps. To fulfill the detector requirements the digitization electronics should have a time resolution ≤ 50 ps and provide a wide dynamic range for charge measurements. The peculiarity of the developed electronics arises from the need to obtain such a time resolution operating in a satellite environment, which implies low-power consumption, radiation hardness, redundancy and high reliability.

© 2003 Elsevier B.V. All rights reserved.

PACS: 29.40.Mc; 07.87.+v; 95.55.Vj; 96.40.De

Keywords: Antimatter research; Electronics; Trigger; Scintillation counters; Space borne experiment

1. Introduction

The PAMELA ToF and [1–2] Trigger electronics is a system composed by nine 6U VME boards. As shown in Fig. 1 six Front End (FE) boards performs the time and charge digitization of the 48 PMTs pulse of the PAMELA ToF. A DSP board gathers data from the FE through serial links and, after digital processing, transfers to the main data-acquisition system. Finally the trigger board receives signals from FE boards to generate the apparatus main trigger, handles the

busy logic of all the subsystems and with the help of about 60 rate counters allows the monitoring of the ToF and other subsystems performances.

2. The FE board

The FE boards receives 8 analog signals from PMTs. For each channel it measures the arrival time of the signal with respect to the trigger pulse and its charge and generates the signals for the trigger. The PMT signal is split into two branches at the input stage to measure time and charge.

In the time section, each PMT anode is coupled to a fast discriminator. To minimize the time-walk effect a double-threshold discriminator is used. The comparator is the AD8598 that has a

*Corresponding author. INFN Sezione di Napoli, Complesso Universitario di Monte S. Angelo, Via Cintia, Naples 80126, Italy.

E-mail address: osteria@na.infn.it (G. Osteria).

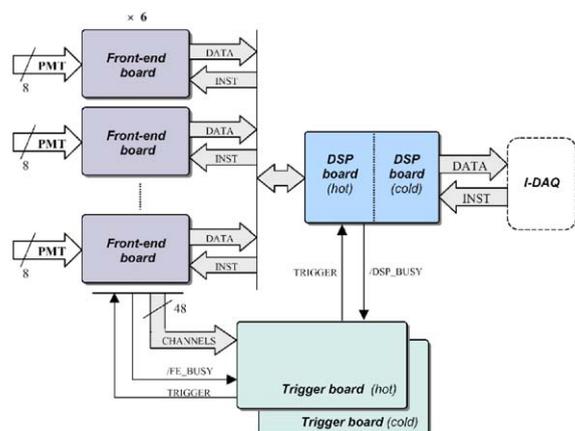


Fig. 1. General electronics layout.

maximum propagation delay of 7 ns. The two thresholds of the comparators can be set by remote through two DAC AD 7303. The discriminated signals are shaped, translated in LVDS standard and sent to the trigger board. The discriminator is a part of a more complex logic that controls a double-ramp Time–Amplitude–Time (TAT) converter with a time expansion factor of 200. All the logic needed to control the TAT converter is fully implemented in a low-power, rad-tolerant Actel 54SX08A FPGA.

The amplitude of each PMT pulse is measured with a Charge-to-Time converter. A charge amplifier collects the anode current of the PMT signal and provides an output signal proportional to the total charge. A pulse stretcher charges-up a capacitor at the peak value of the input waveform and then discharges it linearly. Both charge amplifier and pulse stretcher are implemented using a monolithic transistor array CA3127, manufactured by Intersil. The last stage of the Charge–Time converter is a discriminator that generates the digital pulse with a width equal to discharging time of the pulse stretcher.

The digital signal obtained measuring the discharge time of capacitor, coming from time or charge section, is sent to a 100 MHz TDC fully implemented in a Actel 54SX32A FPGA. This is a 8 channel, common start time-to-digital converter. The time measurement is done digitally by counting 100 MHz clock periods generated by an external oscillator. The circuit has a 10 ns resolu-

tion over a time window of 40.95 μ s, which means a 50 ps resolution on a range of 200 ns, taking into account the time expansion factor. Each TDC receives a signal for measuring the time and one for the charge for each channel so the board houses two TDC. The readout and the initialization of the TDCs is performed by a dedicated 54SX32A FPGA which is the interface between the ToF and the DSP boards. The total power dissipation of the board is less than 3 W.

3. The DSP board

To readout the six FE boards of the ToF subsystem an interface DSP board has been developed which collects data from the six boards and transmit it, through the serial link, to the main DAQ. On this boards is present a Digital Signal Processor (Analog Device) ADSP 2187L which collects data and builds the data packet for the main acquisition. An Actel 54SX32A FPGA contains all the state machines needed to decode macro-commands from CPU and to control the interface with DSP, a second Actel controls the data flow with the FE boards. On the same VME board two replicas of the circuit are implemented. To increase the reliability of the system this board has a ‘cold’ version that can be turned on in case of failures of the ‘hot’ one preserving the full functionality of the system.

4. The trigger board

The trigger board receives the 48 signals from ToF system for the main trigger and about 7 signals from other subsystems able to generate autotrigger for particular events. To guarantee synchronization of the data acquisition, the trigger board manages the busy lines coming from each of the PAMELA subsystem for a total of 20 busy lines. All the input and output lines are in the LVDS standard. About 60 rate counters, dead-live time counters and the logic to generate calibration pulse sequences for different subsystems of the apparatus are also implemented on the board. The logic is distributed on 9 Actel 54SX32A FPGAs.

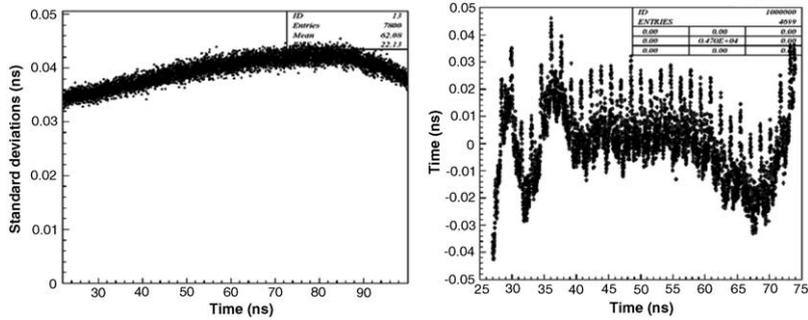


Fig. 2. The time resolution and the integral nonlinearity measurement results.

Control masks select trigger types and allow the selection of failed (noisy or dead) ToF channels. The pattern of the fired channels is generated for each trigger. A DSP (ADSP 2187L) is used to manage the data structure organization and to monitor the rate counters of the ToF channels and other subsystems.

5. The performances

The first test of the performances of the ToF electronics has been performed on the engineering

model of the FE board. Time resolution and integral non linearity have been measured with an AGILENT 81132 pulse generator (RMS jitter of the time base = $15 \text{ ps} \pm 0.001\%$ of the delay). In Fig. 2 results of the two measurements are shown.

References

- [1] O. Adriani, et al., Nucl. Instr. and Meth. A 478 (2002) 114.
- [2] G. Barbarino, et al., Nucl. Phys. B (Proc. Suppl.) 125 (2003) 298.